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FIG.1
RECEIVER BLOCK DIAGRAM

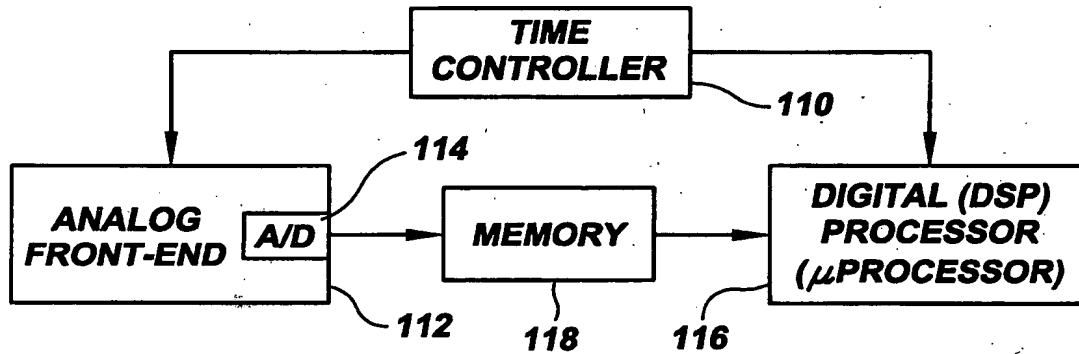


FIG.2
TRANSMITTER BLOCK DIAGRAM

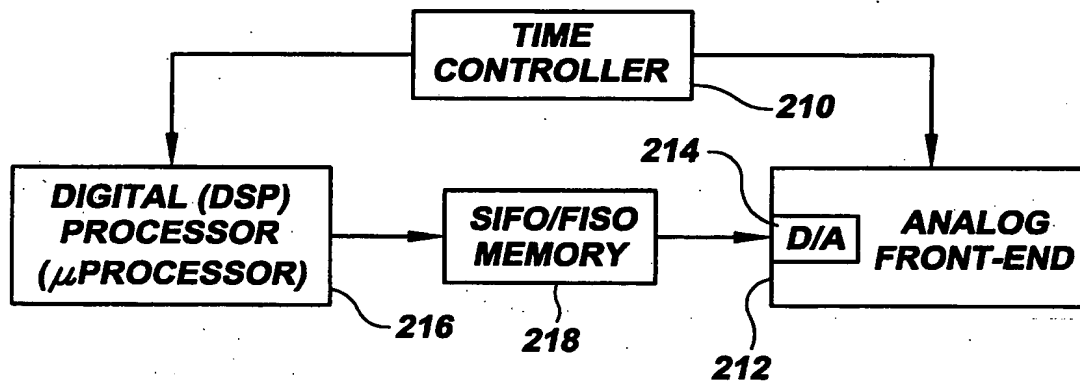


FIG.3 TIME-INTERLEAVED RECEIVER ARCHITECTURE. THE TIMING CONTROLLER REGULATES THE RECEIVER OPERATION BETWEEN THE ANALOG RECEIVER FRONT-END CIRCUITRY AND THE BASEBAND PROCESSING. IT ALSO CONTROLS THE MEMORY IN PERFORMING TIME-INTERLEAVING READ/WRITE OPERATIONS.

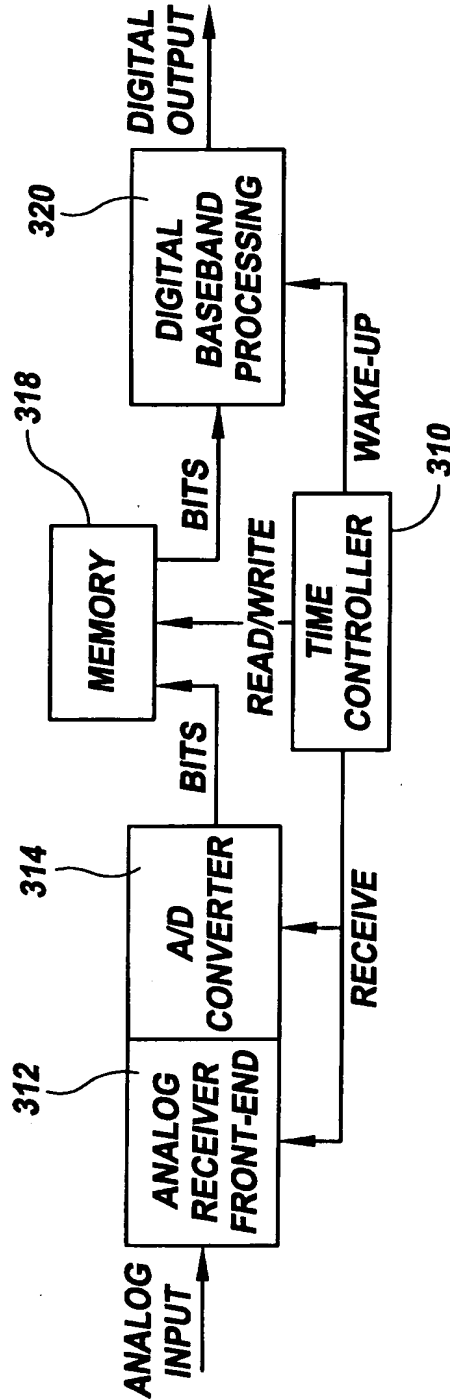


FIG.4 TIME-INTERLEAVED TRANSMITTER ARCHITECTURE. THE TIMING CONTROLLER REGULATES THE TRANSMITTER OPERATION BETWEEN THE ANALOG TRANSMITTER FRONT-END CIRCUITRY AND THE BASEBAND PROCESSING. IT ALSO REGULATES THE MEMORY IN PERFORMING TIME-INTERLEAVING READ/WRITE OPERATIONS.

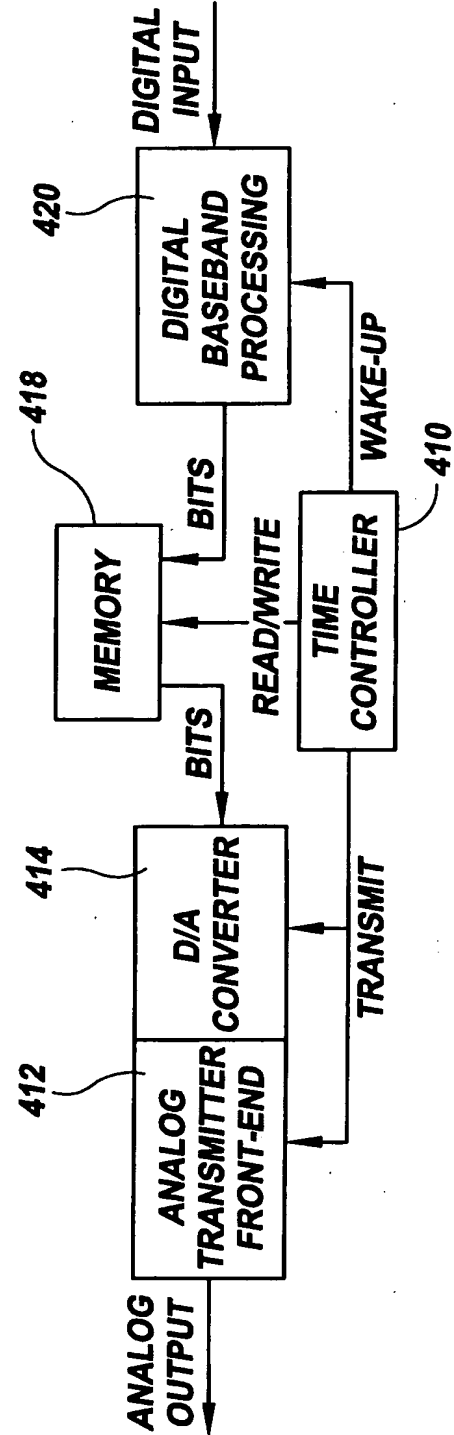
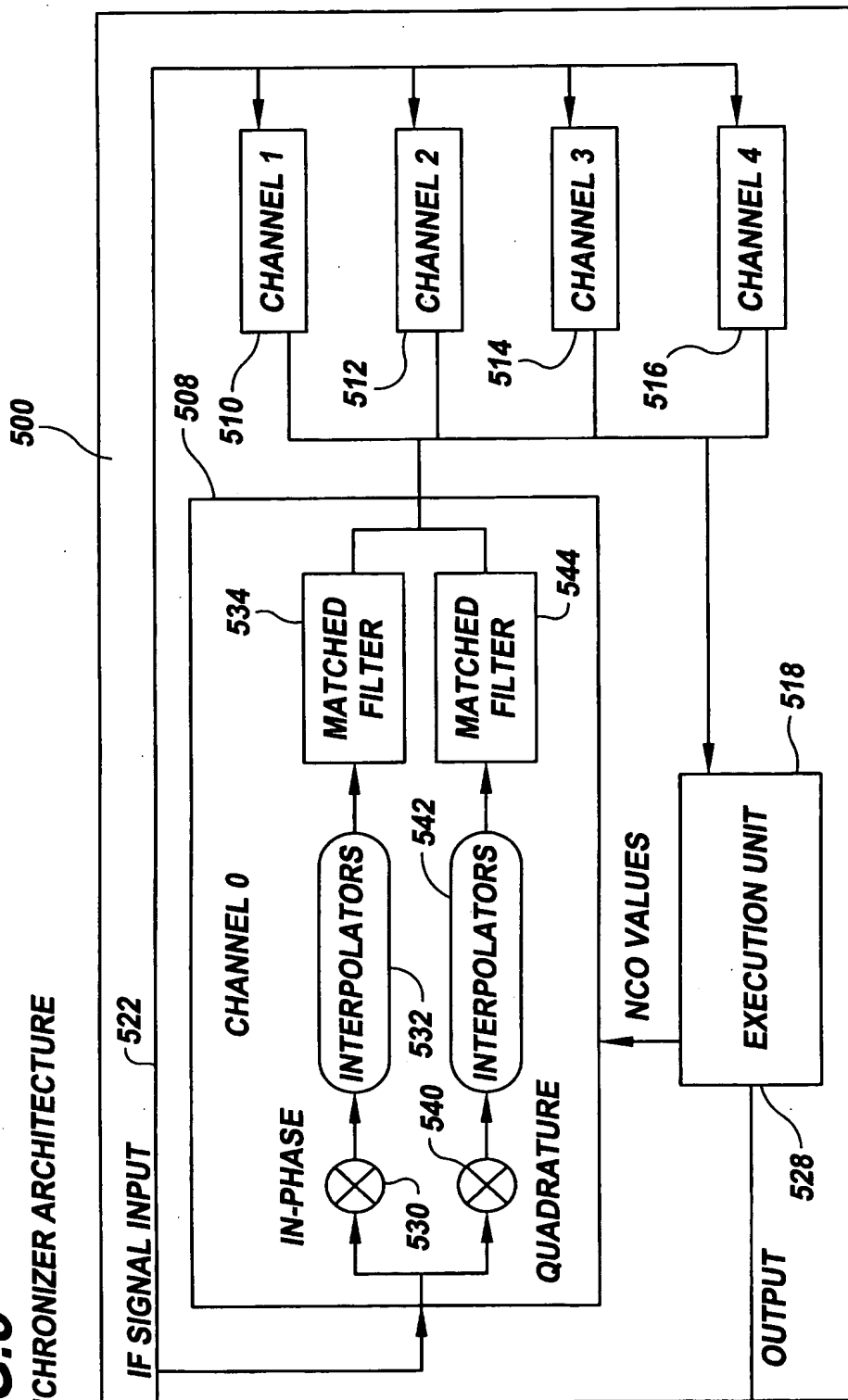




FIG. 5
SYNCHRONIZER ARCHITECTURE



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FIG. 6
EXECUTION UNIT DATAPATH

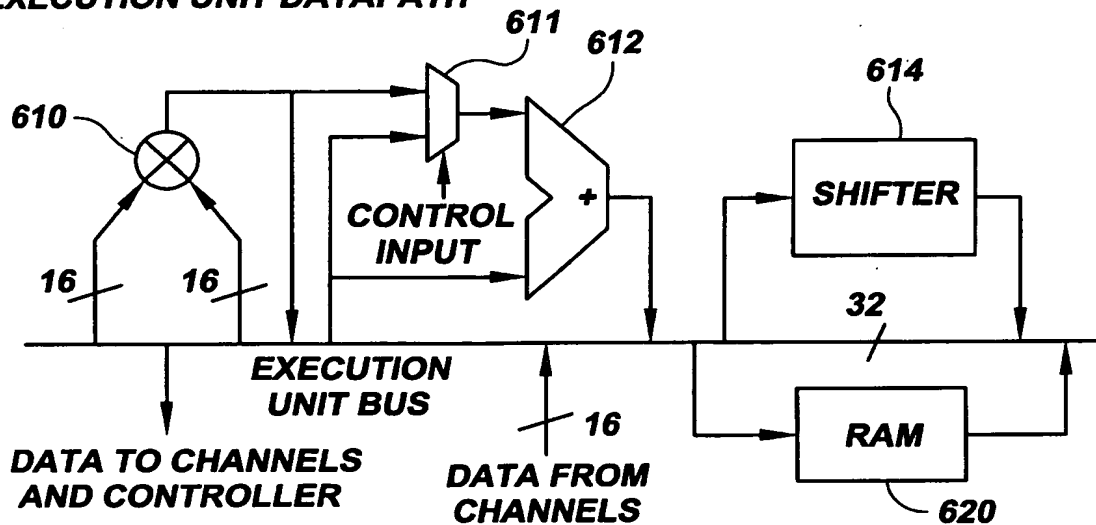


FIG. 7a

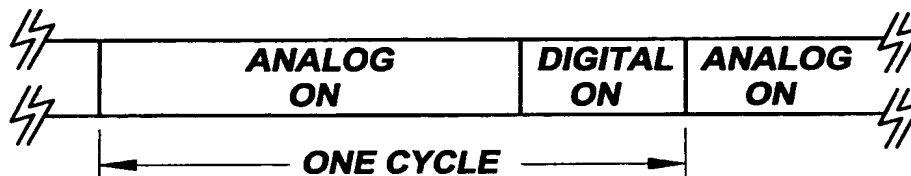


FIG. 7b

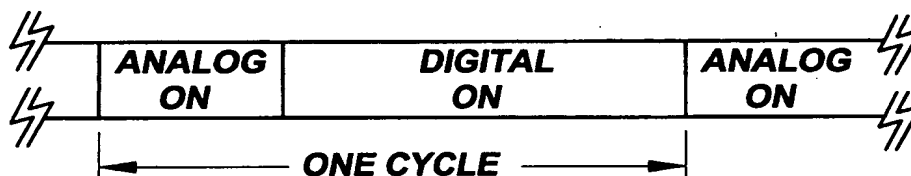


FIG. 7c

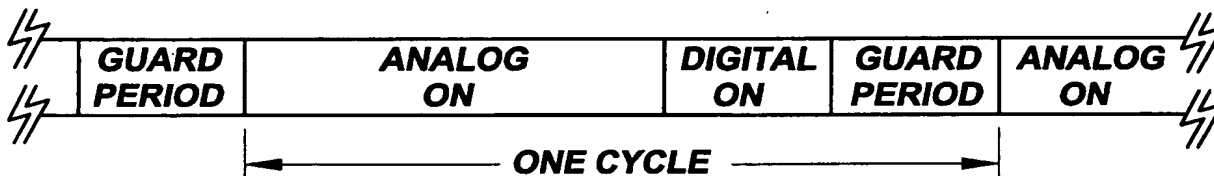


FIG. 7d

